Design and analysis of Three Phase SEPIC Based Inverter Employing Reduced Amount of Switches

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ABSTRACT—The four-switch three-phase (FSTP) inverter has been proposed as an innovative inverter design to reduce the cost, complexity, size, and switching losses of the dc-ac conversion system. Traditional FSTP inverter usually operates at half the dc input voltage; hence, the output line voltage cannot exceed this value. This paper proposes a novel design for the FSTP inverter based on the topology of the single-ended primary-inductance converter (SEPIC). The proposed topology provides pure sinusoidal output voltages with no need for output filter. Compared to traditional FSTP inverter, the proposed FSTP SEPIC inverter improves the voltage utilization factor of the input dc supply, where the proposed topology provides higher output line voltage which can be extended up to the full value of the dc input voltage. The integral sliding-mode control is used with the proposed topology to optimize its dynamics and to ensure robustness of the system during different operating conditions. Derivation of the equations describing the parameters design, components ratings, and the operation of the proposed SEPIC inverter is presented in this paper. Simulation model and experimental setup are used to validate the proposed concept. Simulations and experimental results show the effectiveness of the proposed inverter.

Index Terms—Four-switch three-phase inverter (FSTP), integral sliding-mode control, single-ended primary-inductance converter (SEPIC) converter, sliding-mode control.

INTRODUCTION:

PREVIOUSLY, the conventional six-switch three-phase (SSTP) two-level voltage source inverter (VSI) has found widespread industrial applications in different forms such as motor drives, renewable energy conversion systems, and active power filters. However, in some low power range Applications, reduced switch count inverter topologies are considered to alleviate the volume, losses, and cost. Some research efforts have been directed to develop inverter topologies that can achieve the aforementioned goal. The results obtained showed that it is possible to implement a three-phase inverter with only four switches [1]. In four-switch three-phase (FSTP) inverter, two of the output load phases are maintained from the two inverter legs, while the third load phase is fed from the dc-link at the middle point of a split-capacitor bank as shown in Fig. 1. Recently, the FSTP inverter has attracted the most interests regarding its performance, control, and applications [2]–[17]. Compared to the traditional SSTP inverter, the FSTP inverter has some advantages such as reduced cost and increased reliability due to the reduction in the number of switches, reduced conduction and switching losses by 1/3, where one entire leg is omitted, and reduced number of interface circuits to supply PWM signals for the switches. The FSTP inverter can also be utilized in fault tolerant control to solve the open/short-circuit fault of the SSTP inverter [2], [8], [10]. However, there are some disadvantages of the conventional FSTP inverter which should be taken into consideration. Similar to the traditional SSTP inverter, the FSTP inverter performs only buck dc-ac conversion. Furthermore, the peak phase voltage of the FSTP inverter is reduced to \( \frac{V_{DC}}{2 \sqrt{3}} \), where it is \( \frac{V_{DC}}{2} \) in the SSTP inverter. In order to boost up the phase voltage of the FSTP inverter to that of SSTP inverter, the typical solution is to insert a dc–dc boost converter between the dc input source and the FSTP inverter. However, this adds significant complexity and hardware to the power conversion system and wastes the merits of the reduced switch count. Also, the FSTP inverter topology is not symmetrical; while two load-phases are directly fed from the two inverter legs, the third load-phase is connected to the center tap of split
dc-link capacitors. This forces the current of the third phase to circulate through the dc-link capacitors; hence, a fluctuation will inevitably appear in the two capacitors' voltages, which correspondingly distorts the output voltage [18]. Moreover, if the dc-link split-capacitors have not equal values, there is a possibility of over modulation of the pulse-width modulation process in order to compensate this dilemma [16].

This paper proposes a novel design of the FSTP inverter topology based on the single-ended primary inductance converter (SEPIC). The SEPIC converter is a fourth-order nonlinear system that is extensively used in step-down or step-up dc–dc switching circuits, photovoltaic maximum power point tracking [19], [20], [21], and power factor correction circuits [22], [23] due to its promising features as the no inverting output voltage buck-boost capability and lower input current ripple content. Based on the aforementioned advantages, SEPIC converter has been recently researched by scholars in various topologies in many diversified studies [19]-[35]. Although the proposed FSTP SEPIC inverter has not a voltage boost capability, it can produce an output voltage higher than that of the conventional FSTP VSI by a factor of two, which improves the voltage utilization factor of the input dc supply. Another attractive feature of the proposed SEPIC inverter is that the output voltage is a pure sinusoidal wave, therefore reducing the filtering requirements at the output stage. Also, there is no vital need to insert a dead-band between the same-leg switches, which significantly reduces the output waveform distortion and gain nonlinearity.

Fig. 2: Basic approach to achieve dc–ac conversion with four switches using two SEPIC dc–dc converters. (a) Reference output voltage of the first converter. (b) Reference output voltage of the second converter.

II. PROPOSED FSTP SEPIC INVERTER AND ITS PRINCIPLE OF OPERATION:

The proposed FSTP SEPIC inverter consists of two SEPIC converters, and achieves dc–ac conversion as explained in Fig. 2 by connecting two phases of the three-phase load to the output of two dc–dc SEPIC converters which are sinusoidally modulated Fig. 3. Bidirectional SEPIC converter. Fig. 4. Proposed FSTP SEPIC inverter. [36], while the third phase is directly connected to the input dc source. Both SEPIC dc–dc converters produce a dc-biased sinusoidal wave output, so that each converter produces a unipolar voltage. To generate three-phase balanced load voltages, the sinusoidal modulation of each converter is 120° shifted and the dc-bias is exactly equal to the input dc voltage. Since the load is connected differentially across the two converters and the dc input supply, thus, whereas a dc bias appears at each end of the load with respect to ground, the differential dc voltage across the load is zero and the voltage generated across the load is bipolar voltage, which necessitates the dc–dc SEPIC converters to be current bidirectional. The bidirectional SEPIC dc–dc converter is shown in Fig. 3, while the detailed configuration of the proposed FSTP SEPIC dc–ac inverter is shown in Fig. 4. As shown in Fig. 3, the
bidirectional SEPIC converter includes dc input voltage $V_{DC}$, input inductor $L_1$, two complementary bidirectional power switches $S_1$, $S_2$, coupling capacitor $C_1$, output inductor $L_2$ and output capacitor $C_2$ feeding a load resistance $R_o$. SEPIC operation core implies charging the inductors $L_1$ and $L_2$ during the ON state of the switching period taking the energy, respectively, from the input source and from the coupling capacitor $C_1$, and discharging them simultaneously into the load through the bidirectional switch $S_1$ during the OFF state of the switching period. The output voltage of the SEPIC dc–dc converter may be less or more than the input voltage depending on the duty cycle.

III. CONTROL STRATEGY

A robust control strategy is required to drive the proposed FSTP SEPIC inverter. This is due to the fact that the voltage of one of the three output phases with respect to the common point is equal to the input dc voltage. Thus, any deviation in the output voltage of the two SEPIC dc–dc converters from the desired dbiased sine-wave reference leads to a significant unbalance in the three-phase output line voltages.

3.1 SEPIC Modelling

To design a robust controller, a precise modeling is necessary. The conventional SEPIC converter has a complex model of fourth order, which is derived from the four passive components. This complex high-order system increases the difficulty of obtaining a precise model. The best suitable mathematical model for the application of sliding-mode control (SMC) to the SEPIC is to use a nonlinear (large signal) state space representation. The converter is controlled through two complementary switches, having the control signal as its duty cycle, and is assumed to operate in continuous conduction mode (CCM). Hence, there are two state space representations during both ON and OFF states of the switch. The equivalent circuits of the SEPIC converter during ON and OFF states.

![Fig 3: Bidirectional SEPIC converter.](image1)

![Fig4: Proposed FSTP SEPIC inverter.](image2)

![Fig5: SEPIC equivalent circuit for (a) switch ON and (b) switch OFF.](image3)

3.2 Sliding Mode Control

SMC is a nonlinear control theory which extends the properties of hysteresis control to multivariable environments. It is able to constrain the system status to follow trajectories which lie on a suitable surface in the state space (the sliding surface) [37]–[40]. The main advantages of SMC are the fast dynamic response and the guarantee of stability and robustness for large variations of system parameters and against perturbations [37]. Moreover, given its flexibility in terms of synthesis, SMC is relatively easy to be implemented compared to other types of nonlinear control. However, its application to power converters should be studied for each converter separately. As a control method, SMC has been applied to basic dc–dc converters [41], [42] and complex converters [37], [43], [44]. Although most authors mention the generalization of their developed methods to other high-order converters,
this does not imply to all converters because the difference in circuit topology completely changes the system’s behaviour even if it is of the same order [45].

3.3 Sliding Surface

Although the output voltage \( v_C \) 2 of each SEPIC converter is the final control target, it will be impossible for the closed-loop controlled system to reach stable motion on the sliding surface if \( v_C \) 2 is only selected to be the direct control target, thus the other variables should be chosen. Then, it is proposed to increase the number of state variables as low as possible in the sliding surface. To avoid a large number of tuning gains, a surface containing the input current in addition to the output voltage could be chosen. Where coefficients \( a_1 \) and \( a_2 \) are gains, while \( e_1 \) and \( e_2 \) are the feedback errors of the state variables \( i_L \), and \( v_C \) 2, respectively. The reason for choosing \( i_L \) instead of \( i_L \) is to allow the sliding surface to directly control the input of each converter in addition to its output, which is more stable than the other cases. At an infinitely high switching frequency, the SMC will ensure that both input inductor current and output capacitor voltage are regulated to follow exactly their instantaneous references \( i_L \) ref and \( v_C \) ref, respectively. However, in the case of finite frequency or fixed frequency SMCs, the control is imperfect, where steady-state errors exist in both inductor current and output capacitor voltage. A good method for suppressing these errors is to introduce an additional integral term of the state variables into the sliding surface. Therefore, an integral term of these errors is introduced into the SMC as an additional controlled state-variable to reduce these steady-state errors. This is commonly known as integral sliding-mode control (ISMC).

**IV. SIMULATION RESULTS:**

The proposed FSTP SEPIC inverter has been designed, simulated, and tested to validate its overall performance. The simulations have been done using MATLAB/SIMULINK to validate the analytical results, and to prove the robustness of the recommended DISM control strategy when applied on the proposed inverter topology via different simulation studies. The output phase voltage of the inverter was set to a peak value of 100-V ac, while the input voltage was kept constant at 200-V dc. The parameters of the proposed FSTP SEPIC inverter for simulation are as summarized in the last section. A. Simulation The performance of the proposed FSTP SEPIC inverter under the DISM control strategy has been investigated during both normal and step-changed operating conditions. The corresponding simulation results are shown in Figs. 10 and 11. In particular, Fig. 10 shows the performance of the inverter during normal operating conditions, where the output capacitor voltage and the coupling capacitor voltage of both SEPIC converters are shown in Fig. 10(a) and (b), respectively. Fig. 10(a) shows that the output voltages of both SEPIC converters have sinusoidal waveforms shifted by 120° with a dc bias that is exactly equal to the input dc voltage. Fig. 10(b) shows that the average value of the coupling capacitor voltage for both SEPIC converters is equal to the value of the input dc voltage. The current of both input and output inductors for each SEPIC converter is shown in Fig. 10(c) and (d), respectively. Fig. 10(c) shows that the simulated waveforms of the input inductor currents for both SEPIC converters are consistent with those obtained by equation (7) and shown previously in Fig. 5(a). Fig. 10 (d) shows that the output inductor current has the same waveform of the corresponding load current with superimposed switching ripples. The duty cycle of both SEPIC converters is shown in Fig. 10(e), where they are
varying between approximately 0.12 and 0.65. It should be noted that the waveform of the duty cycle of the SEPIC converter is similar to that obtained from the buck-boost converter at the same values of input and output voltages. This is due to the fact that both SEPIC and buck-boost converters have the same magnitude of the input/output relationship. The input current of the dc supply is shown in Fig. 10(f), where it is a unidirectional current oscillating around 3 A, which is the correct dc value obtained from equation (10). This oscillation is due to the ripples imposed on the input inductor current of both SEPIC and ripples of phase-A current. The three-phase output voltages and load currents of the inverter are shown in Fig. 10(g) and (h), respectively, where the output voltages are well regulated without any filtering requirements. Fig. 11 shows the performance of the inverter during step-changed operating conditions, where Fig. 11(a) exhibits the performance of the inverter under a step change in the load reference voltage from 50 to 100% with doubled frequency, which simulates voltage/frequency control of a three-phase induction motor. Fig. 11(b) shows the performance of the inverter when the load current is changed from 50 to 100%, where the load current has been doubled significantly but the output voltage is almost immediately compensated confirming the robustness of the DISMC.

Fig 8: Proposed simulation diagram of Sepic converter

(b) (c) (d) (g)
V. CONCLUSION:

A dc–ac FSTP SEPIC-based inverter is proposed in this paper. The proposed inverter improves the utilization of the dc bus by a factor of two compared to the conventional FSTP voltage source inverter. Also, it can produce three-phase output voltages that are pure sinusoidal waves without a need for an output filter. Unlike conventional FSTP inverter, the proposed inverter does not suffer from the problems of voltage fluctuation across the dc link split-capacitors, as the third phase load current is directly drawn from the dc source without circulation in any passive component. An SMC with fixed switching frequency was designed and applied to the proposed SEPIC inverter with two different sliding surfaces called integral sliding-mode and double integral sliding-mode (DISMC). It was found that compared to ISMC, the DISMC can eliminate the steady-state error of the state variables by adding double-integral term of these errors in the sliding surface. Simulation and experimental results verified the performance of the proposed inverter with the recommended control strategy.

REFERENCES


