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(24,12) EXTENDED GOLAY CODE BASED AN EFFICIENT SINGLE AND DOUBLE-ADJACENT ERROR CORRECTING PARALLEL DECODER

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ABSTRACT: - An efficient algorithm and the VLSI-architecture for fast soft-decision permutation decoding of the (24,12) extended Golay code are presented. The new decoding technique consists of an optimized permutation decoding with kogge stone parity weight measurement. The idea is to implement a fast parallel decoder to correct the most common error patterns (single and double adjacent) and use a slower serial decoder for the rest of the patterns. In this brief, it is shown that the same scheme can be efficiently implemented for the (24,12,8) Golay code. In this case, the properties of the Golay code can be exploited to implement a parallel decoder that corrects single- and double-adjacent errors that is faster and simpler than a single-error correction decoder. The binary Golay code (*G*23) and extended binary Golay code (*G*24) are implementation in Spartan-3, Virtex-2 and Virtex-2p high speed with low-latency architecture.

Keywords: - Binary Golay Code (23, 12, 7), Extended Golay Code (24, 12, 8), Kogge Stone Adder, Weight
Measurement Unit.

I. INTRODUCTION

With the rapid growth of digital communications, such as Digital Audio Broadcasting (DAB) and ATM systems, increased data rate and advanced error control coding techniques are required. Thus, the parallelism inherent in the decoding algorithm and the area-efficient high-speed VLSI architectures must be exploited. The (24,12,8) extended Golay code is a well- known error-correcting code, which has been successfully applied in several existing communication systems to improve the system bit-error-rate (BER) performance. One goal of this research was to provide a strong error protection for the important head information in the transmission of the high quality compressed music signal of the DAB system. The parallel Golay decoder can be, of course, used generally to protect the data transmission or storage against channel errors for high speed data processing. A number of soft-decision decoding of the (24,12) binary Golay code were intensively investigated in the last few years and detailed analysis of computational complexity were discussed. However, none of these algorithms have been realized efficiently with parallel VLSI circuits. This paper introduces a full parallel permutation decoding technique with look-ahead error-correction and a fast soft-decision decoding for (24, 12, 8) extended Golay code. The area-efficient parallel VLSI architectures and the computer simulation results are also presented.

The look-up table used in this improved algorithm consists of syndrome patterns and corresponding error patterns which have one to three errors occurred in the message block of the codeword. Then the look-up table contains only 25 syndrome patterns and corresponding error patterns. Suppose that there are only three orless errors occurred in (15, 5 ,7) BCH codeword. Due to the latter part of H is a 10x10 identity matrix and S = eHT, if the weight of S w(S)≤3, it means at most three errors only occurred in the parity check block and the location of 1 in S is just the error location in the parity check block. Then shift the syndrome right 5 bits to form a 15-bit length word and minus (modulo 2) the received codeword to decode. If w(S) ≥ 4, it means at least one error occurred in the message block. First, the syndrome minus (modulo 2) all syndrome patterns in the table to obtain the difference and compute the weight of these difference, respectively.

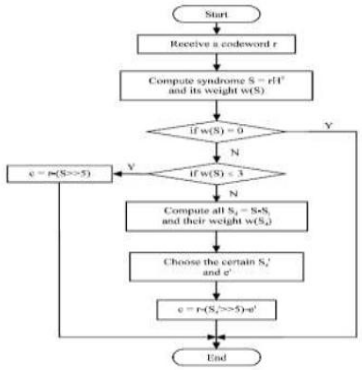

Figure 1: Flow Chart of Golay Code

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II. EXISTING SEC-DAEC PARALLELDECODER

The existing system consist of an encoding-decoding scheme which encodes 12 bit data into 24 bit data by adding 12 check bits to the input. Single and double adjacent (DAEC) errors can be detected and corrected by the use of these extra check bits. The existing SEC-DAEC decoders are similar to SEC decoders but they need to check also the syndrome values that correspond double adjacent errors. This requires roughly doubling the number of comparisons. Then, the correction of each bit is triggered by three syndrome values (the single bit and the two double adjacent). This results in a decoder that is significantly more complex than a simple SEC decoder. Each error has a unique syndrome value, which leads to detection and correction of errors within the range.

The parallel decoder as discussed before has the objective of correcting single and double-adjacent bit errors. The first step is to place the bits in the memory such that data and parity bits are interleaved. This interleaving has no impact on memory performance, as it is a simple remapping of the bits when they are read from or written to the memory.
The requirement for SEC is that the columns must be different. Therefore, it would seem possible to use a subset of the parity bits to decode single errors. However, since the code can correct 3 errors, we want to assure that the single-error parallel decoder does not introduce erroneous corrections in the presence of multiple bit errors. For example, if we use an SEC-DAEC code with a minimum length of four, a triple error can cause a miss-correction in the SEC-DAEC decoding phase. A 4-bit error may not be even detected by the SEC-DAEC decoder. Therefore, the full syndrome is used for comparisons in all the situations to ensure that triple errors do not trigger mis-corrections and 4-bit errors are detected.

III . GOLAY CODE

The Binary Golay code is represented as (23, 12, 7) that depicts that length of codeword is 23 bits, while message is of 12 bits and the minimum distance between two binary Golay codes is 7.

$$A=\begin{bmatrix}0&1&1&0&1&1&1&1&1&1&1&1\\1&1&0&1&1&1&1&1&1&1&1&0\\1&0&1&1&1&1&1&1&1&1&0&1\\1&0&1&1&1&0&0&0&1&0&1&1\\1&1&1&1&0&0&0&1&0&1&1&0\\1&1&1&0&0&0&1&0&1&1&0&1\\1&1&0&0&0&1&0&1&1&0&1&1\\1&0&0&0&1&0&1&1&0&1&1&1\\1&0&0&1&0&1&1&0&1&1&1&0\\1&0&1&0&1&1&0&1&1&1&0&0\\1&1&0&1&1&0&1&1&1&0&0&0\\1&0&1&1&0&1&1&1&0&0&0&1\end{bmatrix}$$

A Galois field (GF) is necessary to construct binary codes. In general, binary field is denoted by GF (2), which supports different binary arithmetic operations. The generation of coding sequence needs a generator polynomial. The possible generator polynomials [13] over GF (2) for Golay (23, 12, 7) code are $x11 + x10 + x6 + x5 + x4 + x2 + x1$ and $x11+x9+x7+x6+x5+x1+1$. In this brief, AE3h is considered as the characteristic polynomial. The remainder of the long division gives the required check bits. Finally, appending the generated check bits with the message gives us the extended Golay codeword. The extended Golay code (24, 12, 8) can be generated by appending a parity bit with the binary Golay code or using a generator matrix *G*, which is defined as [*I*, *B*], where *I* denotes an identity matrix of order 12.

Encoder And Decoder

The first byte of the ROM code is a cyclic redundancy check. If a Golay code is calculated from the following 12 message bits, then agreement with this value implies that the ROM code is error-free. Although this does not have to be used in simple applications. The theory behind this is rather difficult, but is basically working with polynomials with binary numbers as coefficients--that is, 1 or 0. The xor function is the only linear function of two bits. This shift register corresponds to the polynomial x8 + x5 + x4 + 1. It is easy to emulate the shift register in software, although the PIC can only set, clear or test bits, not move them or do operations with them.

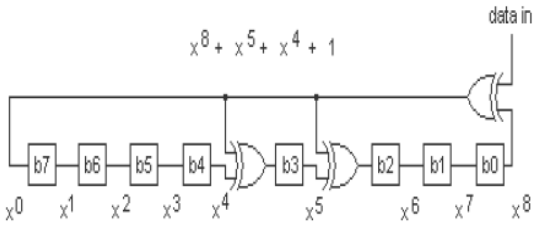

Figure 2: Block Diagram of Encoder for Golay Code

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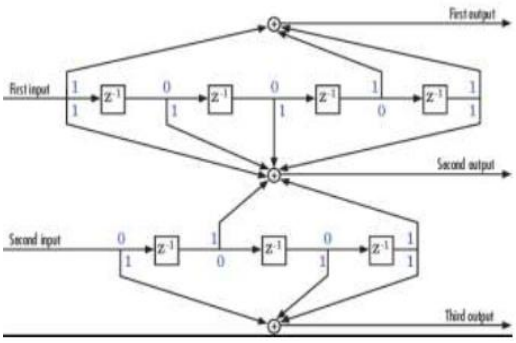

Figure 3: Decoder for Golay code

In this brief, AE3h is considered as the characteristic polynomial. The carry-over of the long division gives the required check bits. Finally, appending the generated check bits with the message gives us the extended Golaycodeword. The extended Golay code (24, 12, 8) can be executed by appending a parity bit with the binary Golay code or using a generator matrix G, which is defined as [I, B], where I denotes an identity matrix.

The Steps required to Accomplish the Encoding Procedure are Enlisted as Follows

1.A characteristic polynomial $G(x)$ is chosen forcheck bits execution.

2.11 zeros are appended to the right of message $M(x)$,like that resultant polynomial $P(x)$ participates inlong division process with $G(x)$.

3.The remainder bits except the most significant bit(MSB) resulted at the end of the division executionare the check bits for G23.Appending check bitswith the message gives us the encoded Golay (23,12, 7) Codeword

4.A parity bit is added to convert the binary GolayCode into showed as a binary Golay Code (24, 12,8). If the weight of binary Golay Code is even, thenparity bit 0 is appended, otherwise 1 is appended.

example of check its generation

An example of GolayCodeword generation based on the encoding algorithm is shown in Fig. 1. Let us say, the data to be encoded is A27h. Hence, $M(x)$ = A27h and $P(x)$ in binary format is showed as 1010 0010 0111 0000 0000 000. Finally, the generated check bits in hexadecimal format are 435h. Hence, the encoded codeword for the data bits (A27h) is A27435h. This is a binary GolayCodeword. To convert it into an extended Golay Code, a parity bit 1 is appended, as weight of A27435h is 11 (odd). Finally, the generated Golay (24, 12, 8) Codeword is (1010 0010 0111 1000 0110 101 1). The validity of the executed Golay Code can be tested by measuring the weight of the code.

IV. PROPOSED METHODOLOGY

In each step during polynomial division, simple binary XOR operation occurs for modulo-2 subtraction. The residual result got at each step during the division process is circularly left shifted by number of leading zeros present in the result. A 12:4 priority encoder is used to detect efficiently the number of leading zeros before first 1 bit in the residual result in each step. A circular shift register is used to shift the intermediate result by the output of priority encoder 2:1 multiplexer is used to select the initial message or the circularly shifted intermediate result. The control signal used for the multiplexer and the controlled subtractor is represented as p, which is bit wise OR operation of priority encoder output. A controlled subtractor is used for loop control mechanism. Initially, one input of subtractor is intimated with 11, which is the number of zeros appended in the first step of the long division process and it gets updated with the content of $R7$ register due to multiplexer chosen after each iteration. The output of the priority encoder is the other input to the subtractor.

After the final iteration, the result of subtractor is zero, which is stored in register $R7$. The register $R6$ is loaded when the content of register $R7$ becomes zero, which depicts the end of the division process and hence the check bits generation process. Architecture for decoding extended Golay Code consist of syndrome measurement, weight measurement, priority encoder and multiplexer to select the register. Satyabrata Sarangi and Swapna Banerjee proposed the structure of weight measurement unit that consists of 2-bit and 3-bit ripple carry adder. Ripple Carry Adder consumes large area and induces more delay as compared to Common Boolean Logic (CBL) adder and Kogge-

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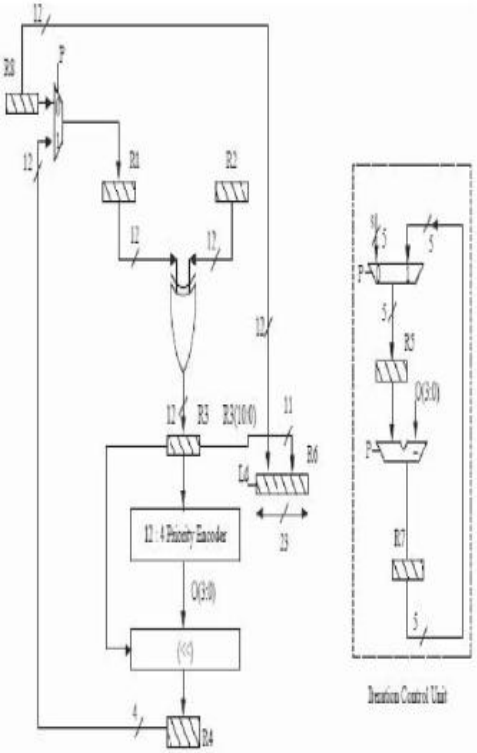
Stone Logic (KSL) adder. Thus to overcome the mentioned problems we will use CBL and KSL in our model.



In this method each error can be identified by finding a value called Syndrome at the decoder. Every error has a unique Syndrome value, which leads to detecting and correcting of errors within the range. By finding the Syndrome value of Tripple adjacent errors (TAEC), we can extend our correctable range to 3 from two. These syndromes values can be calculated by making small changes at the decoder. In the proposed system check bits and syndrome values can be calculated by the use of various circuits. XOR gate is the major gate used in both encoder and decoder. XOR is a circuit made from the basic gates (AND, OR, NOT), which has 5 gates. we can replace these XOR gate by a circuit arrangement which has 4 gates. By using these gate in the system area, power and delay can be upgrade.

V. RESULTS AND DISCUSSION

Error detection and correction helps in transmitting errorless data in a noisy channel. Error detection refers to find errors if any received by the receiver and correction is to correct errors got by the receiver. Different errors correcting codes are there and can be used depending on the properties of the method and the application in which the error correcting is to be intialized. Generally error correcting codes have been classified into Block Codes, Convolutional Codes, Low Density Parity Check Code (LDPC) and Golay Code. The purpose of this thesis is to review the published encoding and decoding models in the literature and to critique their reliability effects. We will try to reduce the area, Maximum Combinational Path Delay (MCPD) of decoding algorithm of Golay Code

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	9	9,312	1%	
Number of 4 input LUTs	4	9,312	1%	
Number of occupied Slices	7	4,656	1%	
Number of Slices containing only related logic	7	7	100%	
Number of Slices containing unrelated logic	0	7	0%	
Total Number of 4 input LUTs	4	9,312	1%	
Number of bonded IOBs	12	232	5%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.71			

```
Setup/Hold to clock clk
------------+------------+------------+------------------+--------+
            |Max Setup to|Max Hold to |                  | Clock  |
Source      | clk (edge) | clk (edge) |Internal Clock(s) | Phase  |
------------+------------+------------+------------------+--------+
biststart   |    0.655(R)|    0.913(R)|clk_BUFGP         |   0.000|
rst         |    1.000(R)|    0.949(R)|clk_BUFGP         |   0.000|
------------+------------+------------+------------------+--------+
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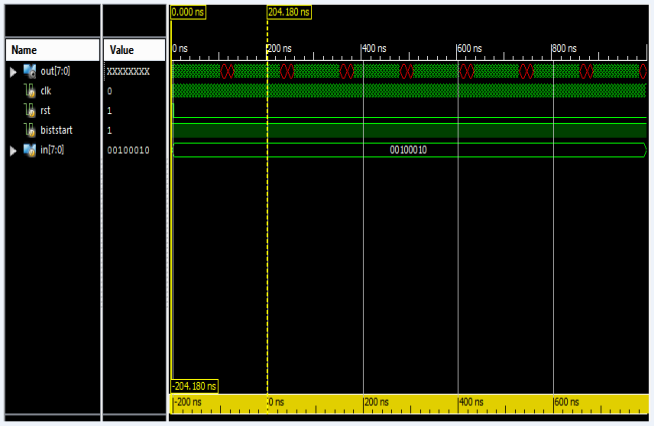

VI. CONCLUSION

The Golay Code and operation for various encoder and decoder is discussed. This encoding and decoding algorithm have been successfully applied to short block codes such as Golay Code in modified proposed methodology. Decoding algorithm consists of syndrome measurement unit, weight measurement unit and weight constraint. the proposed decoder is not only much simpler than a traditional SEC-DAEC

decoder, but also simpler than a standard SEC decoder for the Golay code. To evaluate the benefits of the new decoder, it has been implemented in HDL and mapped to a65-nm library. The results confirm that significant reductions in area, delay, and power consumption can be obtained compared with the traditional SEC-DAEC decoder

REFERENCES:

[1] R. D. Schrimpf and D. M. Fleetwood, *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices*. Singapore:
World Scientific, 2004.

[2] R. C. Baumann, "Soft errors in advanced computer systems," *IEEE Des. Test. Comput.*, vol. 22, no. 3, pp. 258–266, May/Jun. 2005.

[3] C. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," *IBM J. Res. Develop.*, vol. 28, no. 2, pp. 124–134, Mar. 1984.

[4] M. Y. Hsiao, "A class of optimal minimum odd-weight-column
SEC-DED codes," *IBM J. Res. Develop.*, vol. 14, no. 4, pp. 301–395,
Jul. 1970.

[5] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to
a 22 nm design rule," *IEEE Trans. Electron Devices*, vol. 57, no. 7,pp. 1527–1538, Jul. 2010.

[6] P. Reviriego, J. A. Maestro, S. Baeg, S. Wen, and R. Wong, "Protection of memories suffering MCUs through the selection of the
optimal interleaving distance," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 2124–2128, Aug. 2010.

[7] S. Satoh, Y. Tosaka, and S. A. Wender, "Geometric effect of multiple-bit soft errors induced by cosmic ray neutrons on DRAM's," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 310–312, Jun. 2000.

[8] A. Neale and M. Sachdev, "A new SEC-DED error correction code subclass for adjacent MBU tolerance in embedded memory," *IEEE
Trans. Device Mater. Rel.*, vol. 13, no. 1, pp. 223–230, Mar. 2013.

[9] M. A. Bajura *et al.*, "Models and algorithmic limits for an ECC-based approach to hardening sub-100-nm SRAMs," *IEEE Trans. Nucl. Sci.*,
vol. 54, no. 4, pp. 935–945, Aug. 2007.

[10] A. Dutta and N. A. Touba, "Multiple bit upset tolerant memory using a selective cycle avoidance based SEC-DED-DAEC code," in *Proc. IEEE VLSI Test Symp.*, May 2007, pp. 349–354.

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